

<p>Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)</p>	<p>ATTY. DKT. NO. 5732-00100</p> <p>APPLICANT: Chhor et al.</p> <p>FILING DATE: August 13, 2001</p>	<p>SERIAL NO. 09/928,767</p> <p>GROUP: 2818 2876</p>
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U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

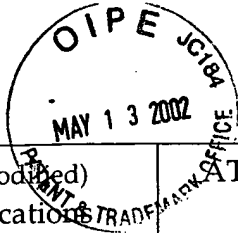
<i>HT</i>	A8	Dipert, "Exotic memories, diverse approaches," EDN Asia, September 2001, pp. 22-33.

EXAMINER: Jared J. Fineman

DATE CONSIDERED: 5/7/2003

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Information Disclosure Statement--PTO 1449 (modified)



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<i>gao</i>	B1	3,414,892	12/1968	McCormack et al.			
	B2	3,432,827	3/1969	Sarno			
	B3	4,489,478	12/1984	Sakurai			
	B4	4,500,905	2/1985	Shibata			
	B5	4,535,424	8/1985	Reid			
	B6	4,630,096	12/1986	Drye et al.			
	B7	4,672,577	6/1987	Hirose et al.			
	B8	4,710,798	12/1987	Marcantonio			
	B9	4,811,082	3/1989	Jacobs et al.			
	B10	5,001,539	3/1991	Inoue et al.			
	B11	5,089,862	2/1992	Warner, Jr. et al.			
	B12	5,160,987	11/1992	Pricer et al.			
	B13	5,191,405	3/1993	Tomita et al.			
	B14	5,202,754	4/1993	Bertin et al.			
	B15	5,266,912	11/1993	Kledzik			
	B16	5,283,468	2/1994	Kondo et al.			
	B17	5,398,200	3/1995	Mazur� et al.			
	B18	5,422,435	6/1995	Takiar et al.			
	B19	5,426,566	6/1995	Beilstein, Jr. et al.			
	B20	5,434,745	7/1995	Shokrgozar et al.			
	B21	5,453,952	9/1995	Okudaira et al.			
	B22	5,455,445	10/1995	Kurtz et al.			
	B23	5,468,997	11/1995	Imai et al.			
	B24	5,481,090	1/1996	Senock et al.			
	B25	5,481,133	1/1996	Hsu			
	B26	5,495,398	2/1996	Takiar et al.			
<i>gao</i>	B27	5,502,289	3/1996	Takiar et al.			

EXAMINER: *Jared J. Trueman*

DATE CONSIDERED: *5/7/2003*

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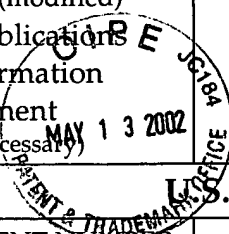
EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<i>gjt</i>	B28	5,523,622	6/1996	Harada et al.			
	B29	5,523,628	6/1996	Williams et al.			
	B30	5,552,963	9/1996	Burns			
	B31	5,561,622	10/1996	Bertin et al.			
	B32	5,581,498	12/1996	Ludwig et al.			
	B33	5,585,675	12/1996	Knopf			
	B34	5,612,570	3/1997	Eide et al.			
	B35	5,654,220	8/1997	Leedy			
	B36	5,693,552	12/1997	Hsu			
	B37	5,696,031	12/1997	Wark			
	B38	5,703,747	12/1997	Voldman et al.			
	B39	5,780,925	7/1998	Cipolla et al.			
	B40	5,781,031	7/1998	Bertin et al.			
	B41	5,801,437	9/1998	Burns			
	B42	5,915,167	6/1999	Leedy			
	B43	5,969,380	10/1999	Seyyeddy			
	B44	5,976,953	11/1999	Zavracky et al.			
	B45	5,985,693	11/1999	Leedy			
	B46	6,057,598	5/2000	Payne et al.			
	B47	6,072,234	6/2000	Camien et al.			
	B48	6,087,722	7/2000	Lee et al.			
	B49	6,133,640	10/2000	Leedy			
	B50	6,185,122	2/2001	Johnson et al.			
	B51	6,197,641	3/2001	Hergenrother et al.			
	B52	6,208,545	3/2001	Leedy			
	B53	6,281,042	8/2001	Ahn et al.			
<i>gjt</i>	B54	6,291,858	9/2001	Ma et al.			

EXAMINER: *Greg J. J. J. J.*

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225	B55	6,307,257	10/2001	Huang et al.			
	B56	6,314,013	11/2001	Ahn et al.			
	B57	6,322,903	11/2001	Siniaguine et al.			
	B58	6,337,521	1/2002	Masuda			
	B59	6,351,028	2/2002	Akram			
	B60	6,353,265	3/2002	Michii			
225	B61	6,355,501	3/2002	Fung et al.			

U.S. PATENT APPLICATION PUBLICATIONS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
225	B62	2001/0033030	10/2001	Leedy			
	B63	2001/0054759	12/2001	Nishiura			
	B64	2002/0024146	2/2002	Furusawa			
	B65	2002/0027275	3/2002	Fujimoto et al.			
	B66	2002/0030262	3/2002	Akram			
225	B67	2002/0030263	3/2002	Akram			

FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
225	B68	0 073 486	3/1983	EP			—
	B69	0 387 834	9/1990	EP			—
	B70	0 395 886	11/1990	EP			—
	B71	0 516 866	12/1992	EP			Yes, Abstract Only
	B72	0 606 653	7/1994	EP			—
	B73	0 644 548	3/1995	EP			—
	B74	0 800 137	10/1997	EP			—
225	B75	60-22352	2/1985	JP			Yes, Abstract Only

EXAMINER: James G. Trueman

DATE CONSIDERED: 5/7/2003

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>gjo</i>	B76	61-222216	10/1986	JP			Yes, Abstract Only
<i>gjo</i>	B77	63-52463	3/1988	JP			Yes, Abstract Only
<i>gjo</i>	B78	94/26083	11/1994	WO			—

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<i>gjo</i>	B79	Akasaka, "Three-dimensional integrated circuit: technology and application prospect," Microelectronics Journal, Vol. 20, Nos. 1-2, 1989, pp. 105-112. <i>No month.</i>
	B80	Sakamoto, "Architecture des Circuits à Trois Dimensions," Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, pp. 16-29. <i>No month.</i>
	B81	Akasaka, "Three-Dimensional IC Trends," Proceedings of the IEEE, Vol. 74, No. 12, ^{December} 1986, pp. 1703-1714.
	B82	Pein et al., "Performance of the 3-D PENCIL Flash EPROM Cell and Memory Array," IEEE Transactions on Electron Devices, Vol. 42, No. 11, ^{November} 1995, pp. 1982-1991.
	B83	Jokerst et al., "Manufacturable Multi-Material Integration: Compound Semiconductor Devices Bonded to Silicon Circuitry," SPIE Vol. 2524, 1995, pp. 152-163. <i>No month.</i>
	B84	Camperi-Ginestet et al., "Vertical Electrical Interconnection of Compound Semiconductor Thin-Film Devices to Underlying Silicon Circuitry," IEEE Photonics Technology Letters, Vol. 4, No. 9, ^{September} 1992, pp. 1003-1006.
	B85	Lomatch et al., "Multilayered Josephson junction logic and memory devices," SPIE Vol. 2157, ^{January} 1994, Abstract Only, 2 pgs.
	B86	Lu, "Advanced cell structures for dynamic RAMs," IEEE Circuits and Devices, Vol. 5, No. 1, ^{January} 1989, Abstract Only, 2 pgs.
	B87	Sakamoto, "Architecture of three dimensional devices," Bulletin of the Electrotechnical Laboratory, Vol. 51, No. 1, 1987, Abstract Only, 2 pgs. <i>No month.</i>
	B88	"Wide application of low-cost associative processing seen," Electronic Engineering Times, ^{August} 1996, 6 pgs.
	B89	"Interconnects & Packaging," Electronic Engineering Times, ^{June} 1996, 8 pgs.
	B90	"Closing in on gigabit DRAMs," Electronic Engineering Times, ^{November} 1995, 4 pgs.
	B91	"Module Pact Pairs Cubic Memory with VisionTek," Semiconductor Industry & Business Survey, Vol. 17, No. 15, ^{October} 1995, 2 pgs.
	B92	Flaherty, "Layers of BST materials push toward 1Gbit DRAM," Electronic Times, ^{October} 1995, 3 pgs.
<i>gjo</i>	B93	Santoni, "Technologies Will Pursue Higher DRAM Densities," Electronic News, ^{December} 1994, 7 pgs.

EXAMINER: *David J. Omenan*

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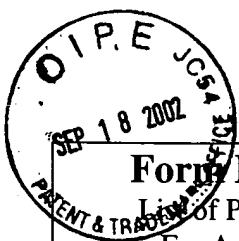
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

225	B94	Weber, "Looking for diverse storage," Electronic Engineering Times, ^{October} 1994, 7 pgs.
	B95	"Special Report: Memory Market Startups, Cubic Memory: 3D Space Savers," Semiconductor Industry & Business Survey, Vol. 16, No. 13, ^{September} 1994, 6 pgs.
	B96	Bindra, "Technique boosts 3D memory density," Electronic Engineering Times, ^{August} 1994, 2 pgs.
	B97	Bindra, "Memory packs poised for 3-D use," Electronic Engineering Times, ^{December} 1992, 4 pgs.
	B98	Derman, "MCMs hit the road," Electronic Engineering Times, ^{June} 1992, 6 pgs.
	B99	Bindra, "IEDM ponders the 'gigachip' era," Electronic Engineering Times, ^{January} 1992, 4 pgs.
	B100	"Tech Watch: 1-Gbit DRAM in sight," Electronic World News, ^{October} 1991, 2 pgs.
	B101	Derman, "MCMs meld into systems," Electronic Engineering Times, ^{July} 1991, 7 pgs.
	B102	Brown, "Systems EEs see future in 3-D," Electronic Engineering Times, ^{September} 1990, 4 pgs.
	B103	Hayashi et al., "A New Three Dimensional IC Fabrication Technology, Stacking Thin Film Dual CMOS Layers," © 1991 IEEE, 4 pgs. <i>No month.</i>
	B104	Tielert, "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic," © 1996 IEEE, pp. 121-124. <i>No month.</i>
	B105	Stern et al., "Design and Evaluation of an Epoxy Three-Dimensional Multichip Module," IEEE Transactions on Components, Packaging, and Manufacturing Technology - Part B, Vol. 19, No. 1, 1996, pp. 188-194. <i>No month.</i>
	B106	Bertin et al., "Evaluation of a Three-Dimensional Memory Cube System," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol. 16, No. 8, 1993, pp. 1006-1011. <i>No month.</i>
	B107	Watanabe et al., "Stacked Capacitor Cells for High-density dynamic RAMs," © 1988 IEEE, pp. 600-604. <i>No month.</i>
	B108	"Stacked Memory Modules," IBM Technical Disclosure Bulletin, Vol. 38, No. 5, ^{May} 1995, 2 pgs.
	B109	"3-D Chip-on-chip Stacking," Semiconductor International, ^{December} 1991, 1 pg.
	B110	Thakur et al., "An Optimal Layer Assignment Algorithm for Minimizing Crosstalk for Three Layer VHV Channel Routing," © 1995 IEEE, pp. 207-210. <i>No month.</i>
	B111	Terrill et al., "3D Packaging Technology Overview and Mass Memory Applications," © 1996 IEEE, pp. 347-355. <i>No month.</i>
	B112	^{May} Sugahara et al., "A Three-Dimensional Static RAM," IEEE Electron Device Letters, Vol. EDL7, No. 5, 1986, pp. 327-329.
	B113	Tielert, "Benefits of Vertically Stacked Integrated Circuits for Sequential Logic," ^{December} © 1996 IEEE, pp. 121-124.
	B114	Akasaka, "Three-Dimensional IC Trends," © 1986 IEEE, pp. 1703-1714. <i>No month.</i>
225	B115	Kurokawa et al., "3-D VLSI Technology in Japan and an Example: a Syndrome Decoder for Double Error Correction," Future Generation Computer Systems, Vol. 4, No. 2, ^{September} 1988, pp. 145-155.

EXAMINER: *James J. Timmerman*

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ATTY. DKT. NO. 5732-00100

SERIAL NO. 09/928,767

APPLICANT: Chhor et al.

GROUP: ~~2818~~
2876

FILING DATE: August 13, 2001

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<i>gld</i>	C1	5,745,407	4/1998	Levy et al.			

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